CBCS SCHEME

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18CS33

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain the construction, working and characteristics of photo diode. **(06 Marks)**
b. With hysteresis characteristics explain the working of Schmitt trigger circuit (Inverting). **(06 Marks)**
c. With a neat circuit diagram and mathematical analysis explain voltage divider bias circuit. **(08 Marks)**

OR

2 a. Explain the working of R-2R ladder D to A converter. **(06 Marks)**
b. Explain successive approximation A to D converter. **(06 Marks)**
c. Show how IC-555 timer can be used as an astable multivibrator. **(08 Marks)**

Module-2

3 a. Find the minimum SOP and minimum POS expressions for the following function using K-map. $f(A, B, C, D) = \sum_m (1, 3, 4, 11) + \sum_d (2, 7, 8, 12, 14, 15)$. **(06 Marks)**
b. What are the disadvantages of K-map method? How they are overcome in Quine Mccluskey method. Simplify following function using Q-M method
$f(A, B, C, D) = \sum_m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$. **(08 Marks)**
c. What is Map-Entered Variable method? Using MEV method simplify following function:
$f(A, B, C, D) = \sum_m (2, 3, 4, 5, 13, 15) + dc(8, 9, 10, 11)$. **(06 Marks)**

OR

4 a. With the help of flow chart explain how to determine minimum sum of products using Karnaugh map. **(06 Marks)**
b. Using Q-M method simplify the following function
$F(A, B, C, D) = \sum_m(2, 3, 7, 9, 11, 13) + \sum_d(1, 10, 15)$. **(08 Marks)**
c. With example explain Petrik's method. **(06 Marks)**

Module-3

5 a. What are hazards in digital circuits? Explain different types of hazards. **(06 Marks)**
b. Implement full subtractor using 3 to 8 decoder and NAND gates. **(06 Marks)**
c. Differentiate between PAL and PLA. Realize following functions using PLA. Give PLA table and internal connection diagram for the PLA (Use as many common terms as possible)
$F_1(1, b, c, d) = \sum_m(1, 2, 4, 5, 6, 8, 10, 12, 14)$
$F_2(a, b, c, d) = \sum_m(2, 4, 6, 8, 10, 11, 12, 14, 15)$ **(08 Marks)**

OR

6 a. What is Multiplexer? Implement following function using 8:1 MUX
$f(A, B, C, D) = \sum_m(1, 2, 5, 6, 9, 12)$ **(08 Marks)**
b. Design Hexadecimal (Binary) to ASCII Code Converter using suitable ROM. Give the connection diagram of ROM. **(06 Marks)**
c. Explain Simulation and testing of digital circuits. **(06 Marks)**

Module-4

7 a. Explain the structure of VHDL program. Write VHDL code for 4 bit parallel adder using full adder as component. **(08 Marks)**

b. Explain the working of SR latch using NOR gates. Show how SR latch can be used for switch debouncing. **(07 Marks)**

c. Differentiate between Latch and Flip Flop. Show how SR flipflop can be converted to D flip flop. **(05 Marks)**

OR

8 a. Derive the characteristics equations for D, T, SR and JK flipflops. **(08 Marks)**

b. Draw the logic diagram of master slave JK flipflop using NAND gates and explain the working with suitable timing diagram. **(07 Marks)**

c. With example explain the syntax of conditional signal assignment statement in VHDL. **(05 Marks)**

Module-5

9 a. What is shift register? Explain the working of 8 bit SISO shift register using SR flip flop. **(06 Marks)**

b. With the help of state graph, state and transition tables and timing diagram explain sequential parity checker. **(06 Marks)**

c. Design a random counter using T flip flops whose transition graph is shown in Fig.Q.9(c). **(08 Marks)**

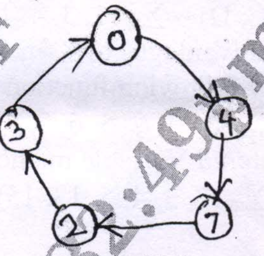

Fig.Q.9(c)

OR

10 a. What is register? Explain how 4 bit register with data, load, clear and clock input is constructed using D flip flops. **(06 Marks)**

b. With a block diagram explain the working of n-bit parallel adder with accumulator. **(06 Marks)**

c. Differentiate between Moore and Melay machines. Analyze following Moore sequential circuit for an input sequence of X = 01101 and draw the timing diagram. **(08 Marks)**

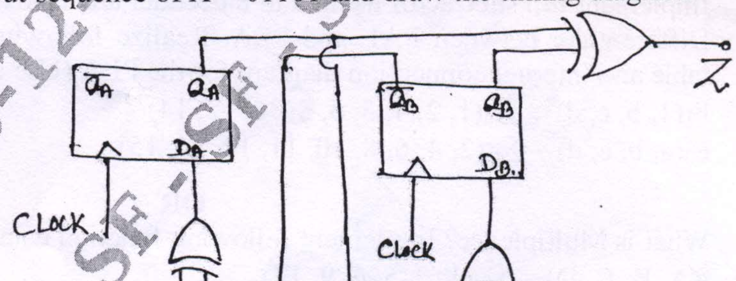

Fig.Q.10(c)

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